REMARKS

Reconsideration of the application is requested. The reference to Uchida (US Pub. 2002/0031882) and in particular figure 14, is not combinable with Applicant's Admitted Prior Art (AAPA) because the admitted prior art describes a single memory cell whereas figure 14 has many circuit sections. For example, in Uchida (US Pub. 2002/0031882) the trench isolation 2 referred to in the Official Action only partially isolates the input/output circuit zone 32. Thus, the active region would be located within the input/output zone 32. Therefore, only the second region 62 is located within the defined active region, as is required by independent claims 1 and 13. The first region 61 is located within the 31 peripheral circuit zone and isolated from the input/output zone 32. Therefore, one can not combine the teaching of AAPA with the cited reference because one teaches a single cell and the other teaches a multiple transistor circuits. One of ordinary skill in the art would not even consider the cited reference, and could not reduce the combination to practice if considered without undue experimentation.

Claim Rejections - 35 USC § 103

"Claims 1-3 and 6-12 are rejected under 35 USC 103(a) as being unpatentable over Uchida (US Pub. 2002/0031882) in view of the Applicant's Admitted Prior Art (AAPA).

In re claim 1, Uchida discloses a process for making a semiconductor device comprising the steps of (Figs 1-15 and related text):

forming an isolation region (Fig 14:2) on an epitaxial layer of a semiconductor substrate (fig. 14:60) to define an active region having a predefined boundary (page 6, paragraph 0080);"

Applicant's Response

As discussed in Uchida the trench isolation 2 referred to in the Official Action only partially isolates the input/output circuit zone 32, and does not define an active region. Even if that was the case, the defined active region would be located within the input/output zone 32. As will be discussed later, the first region and the second region are taught by the application to be located within the defined active region as is required by claim 1.

Claim 1 Rejection - 35 USC § 103
(Continued)

"implanting a first dopant into the epitaxial layer within the active region to create a well (fig. 14:16) of a first type of conductivity (page 6, paragraph 0008);

implanting the first dopant into the well to create a first region (fig. 14:61) and a second region (fig. 14:62) separated from the first region, the first and second regions being implanted across the boundary of the active region and directly spaced apart from each other across the active region and spaced apart from the center of the active region (page 6, paragraph 0087);"

Applicant's Response

As can be seen from figure 14, the P-well 16 is located within the input/output circuit zone 32, and the second region is identified as the buried N-type layer 62 which is also located in the input/output circuit zone 32. The identified first region is shown in figure 14 as the buried N-type layer 61. The Uchida reference is not obvious to Applicant's claims as the identified first region is a buried N-type layer 61 located in a peripheral circuit zone 31 that is separate, distinct and isolated from the active region identified as being defined by the trench isolation 2. Additionally, the first region, the buried n-type layer 61, could not be implanted into the well, as the well is identified as the P-well 16 and the buried N-type layer 61 is located away from the P-well 16, as shown in figure 14.

Claim Rejections - 35 USC § 103
(Continued)

"depositing a polysilicon layer)fig. 4:37) over the active region (page 6, paragraph 0087);

doping the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate (fig. 14:29) over the first and second regions and well (page 6, paragraph 0087); and"

Applicant's Response

As is shown, the buried layer 61 is located under the gates that includes gate electrode

and gate oxide layer 7 and 27 as well as the gate electrode 26 and gate oxide film 6. The buried N-type layer 62 is located under the gates that includes the gate electrode 29 and gate oxide film 66 and gate electrode 28 and gate oxide film 65. Thus, the reference shows a plurality of gates over what the rejection identified as a first region and a second region. This is contrary to what claim 1 claims, as it requires a pattern of a polysilicon layer to create a poly gate over the first and second regions and well. This is just not present in figure 14 of the Uchida reference.

Claim Rejections - 35 USC § 103
(Continued)

"performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by a channel region beneath the poly gate (fig. 14);

Uchida fails to explicitly disclose depositing an oxide layer over the poly gate and active region; etching the oxide layer to create side spacers on each side of the poly gate; and implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the first and second lightly doped regions and the channel region.

AAPA discloses performing a LOCOS operation on an epitaxial layer of a semiconductor substrate to define an active region having a predefined boundary (fig. 3); depositing an oxide layer over the poly gate (fig. 3:1) and active region; etching the oxide

layer to create side spacers (fig. 3: 7, 17) on each side of the poly gate; and implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source (fig. 3:3) and drain (fig. 3:2) regions, the source and drain regions being separated by the first (fig. 3:5) and second (fig. 3:15) lightly doped regions and the channel regions (page 8, 2nd paragraph). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish a CMOS and BICMOS device structures (page 8, 2nd paragraph)."

Applicant's Response

The combination of figure 14 with AAPA would not have been obvious to one of ordinary skill in the art because AAPA defines the structure for a single cell. Figure 14 and the elements relied upon therein, covered a plurality of transistor elements, whereas Applicant's claims are directed to a single memory cell. Therefore, the combination of the plurality of steps used to manufacture different circuit elements with a single element would not have been obvious to one of ordinary skill in the art. However, one of ordinary skill in the art would understand that a memory contains many memory cells that are all manufactured with the same process.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 2, Uchida discloses wherein the process according to claim 1, further including the step of: implanting the second type of dopant into the semiconductor substrate

propr to the step of growing the epitaxial layer (page 4, paragraph [0063] and fig. 1)."

Applicant's Response

Applicant has distinguished his invention over the Uchida reference as well as the combination of Uchida with AAPA. Therefore, claim 2 provides further definition of what Applicant regards as his invention and should be allowed for at least the same reasons as claim 1.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 3, Uchida discloses wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant (fig. 14)."

Applicant's Response

Applicant has distinguished his invention over the Uchida reference as well as the combination of Uchida with AAPA. Therefore, claim 3 provides further definition of what Applicant regards as his invention and should be allowed for at least the same reasons as claim 1.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 6, Uchida discloses wherein the first type of dopant is a P type of dopant and the step of performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant with each of the first and second lightly doped regions and positioned to be in contact with the first and second regions (page 6, paragraphs [0079]-[0084] and fig. 14)."

Applicant's Response

Applicant disagrees with the rejections of claim 6. The buried N-type layer 61 does not come in contact with a locos area. Similar arguments can be made in regard to the buried N-type layer 62. As the paragraphs relied upon in the rejections describe a formation of a plurality of P and N wells and the creation of a buried N-type layer 61 and a buried N-type 62, these areas do not apply to a single transistor cell as is claimed by Applicant's claims. But, rather defines a plurality of transistors that create a input/output circuit zone 32, a peripheral circuit zone 31 and a memory circuit zone 30. Thus, Applicant's invention could not have been ascertained from the Uchida reference.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 7, Uchida discloses wherein the step of: patterning the poly semiconductor layer to create a poly gate (fig. 14:29) includes the step of: patterning the poly gate over the first and second regions (page 6, paragraph [0084] and fig. 14)."

Applicant's Response

Applicant disagrees with the rejection, nowhere is there a pattern of a poly gate that is a single poly gate over the first and second regions, as suggested by the rejection. There are multiple gates over the first region and multiple gates over the second region as was discussed previously in Applicant's response.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 8, Uchida discloses wherein the first type of dopant is a P-type of dopant and the step of: performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N-type dopant with each of the first and second lightly doped regions being positioned not to be in contact with the first and second regions (page 6, paragraphs [0079]-[0084] and fig. 14)."

Applicant's Response

Applicant respectfully disagrees with the rejections made in regard to claim 8. Nowhere is it shown or discussed, regions such as Applicant's 5 and 15 that are claimed and illustrated in figure 5. As was discussed earlier, the buried N-type layer 62 and the buried N-type layer 61 are not under a single gate, so it would be impossible for one of ordinary skill in the art to read Applicant's claims on figure 14.

In fact, according to paragraph 0081, the N-type layer 61 and 62 are formed in the inside of the substrate and not within the P-well 16.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 9, Uchida discloses wherein the step of: "performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N-type dopant (fig. 14);"

Applicant's Response

The element referred to in the rejection is the claimed lightly doped drain regions. Applicant cannot identify any such regions in figure 14.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 10, Uchida discloses wherein the step of: "implanting a heavy dose of second type of dopant comprises the step of: implanting the heavy dose of N type dopant into the first and second lightly doped regions (page 6, paragraphs [0079]-[0084] and fig. 14)."

Applicant's Response

Applicant could not find anywhere in figure 14, on page 6 paragraphs 79-84, the step of implanting the heavy dose of N-type dopant into the first and second lightly doped regions. Thus, claim 10 would not have been obvious to one of ordinary skill in the art.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 11, Uchida fails to explicitly wherein the step of: implanting a heavy dose of second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the channel region; all included the step of: patterning the active area using a first reticle to create a pattern on the active region (page 8, 2nd paragraph and fig. 3)."

Applicant's Response

As explained in paragraph 0056 the buried P-type layer is formed in figure 3. This is part of the steps used to create the peripheral circuit zone for a DRAM circuit. There is no teaching of a second type of dopant between the locos regions, as there are no locos regions shown. There is no teaching of a drain source, nor is there a teaching that the drains regions are separated by the channel regions, none of this is provided in figure 3. In AAPA, Applicant has distinguished independent claim 1 to which claim 11 depends over the cited references. Thus claim 11 should be allowed for at least the same reason.

Claim Rejections - 35 USC § 103
(Continued)

"AAPA discloses wherein the step of: implanting a heavy dose of second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the channel region; all included the step of: patterning the active area using a first reticle to create a pattern on the active region. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish CMOS and BICMOS device structures (page 8, 2nd paragraph).

In re claim 12, Uchida discloses wherein the step of: performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by

a channel region beneath the poly gate included the step of: patterning the active area using the first reticle to create a pattern on the active region (fig. 14)."

Applicant's Response

Applicant has previously distinguished independent claim over the combination of Uchida and AAPA. Claim 12 provides further definition of the steps used to practice Applicant's inventions, and should be allowed for at least the same reasons as those discussed in conjunction with claim 1.

Claim Rejections - 35 USC § 103
(Continued)

"Claims 13-15 and 17-21 are rejected under 35 USC 103(a) as being unpatentable over Uchida in view of the AAPA.

In re claim Uchida discloses a process for making a semiconductor device comprising the steps of (figs. 1-15, and related text):

forming an isolation region (fig. 14:2) on an epitaxial layer to define an active region;"

Applicant's Response

The reference to Uchida defines the isolation regions in paragraph 0086 as: " First, the advantage of the fact that the third embodiment has a triple well structure, will be described. In the third embodiment, the 25 P-well 10 of the memory cell zone 30, the P-well 14 of the peripheral circuit zone 31, and the P-well 16 of the input/output circuit zone 32 and are electrically isolated from each other by means of the N-wells 13, 63 and 15 and the buried

N-type layers 61 and 62." Thus, there are 3 separate isolation regions all of which are isolated from one another.

Claim Rejections - 35 USC § 103
(Continued)

"using the first reticle to create a pattern for implanting a first dopant into the epitaxial layer within the active region to create a well (fig. 14:61) of a first type of conductivity (page 6, paragraphs [0079]-[0084];

using a second reticle to create a pattern for implanting with the first type of dopant into the well to create first region (fig. 14:61) and second regions (fig. 14:62) across the boundary of the active region and spaced directly apart across the active region from each other and spaced apart from the center of the active region (page 6, paragraph [0087]);"

Applicant's Response

As explained in paragraph 0086, quoted above, the N-type layer 61 is part of the isolation for peripheral circuit zone 31and is implanted through N well 13 and P well 14 and N type layer 62 is part of the input/output circuit 32 and is implanted through N well 15 and P well 16. Reference may be made to figure 11. Thus, the buried layers do not meet the claim requirements of : "using a second reticle to create a pattern for implanting with the first type of dopant into the **well** to create first region and second regions across the boundary of the active region and spaced directly apart across the active region from each other and spaced apart from the center of the active region;" (emphasis added) as they are at least not spaced apart from the center of the active region and not implanted in the same well.

Claim Rejections - 35 USC § 103
(Continued)

"depositing a polysilicon layer 9fig. 4:37) over the active region (page 6, paragraph [0084]);

heavily doping with a second dopant the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate (fig. 14:29) (page 6, paragraph [0084]); and

using a third reticle to create a pattern for lightly doping with a second dopant the active region between the LOCOS regions and the poly gate (page 6, paragraphs [0079]-[0084] and fig. 14);"

Uchida fails to explicitly disclose depositing an oxide layer over the poly gate and active region; etching the oxide layer to create side spacers on each side of the poly gate; and using the third reticle to create a pattern for heavily doping with the second dopant the active region between the LOCOS regions and the side spacers.

AAPA discloses performing a LOCOS operation on an epitaxial layer of a semiconductor substrate to define an active region having a predefined boundary (fig. 3); depositing an oxide layer over the poly gate (fig. 3:1) and active region; etching the oxide layer over the poly gate (fig. 3:1) and active region; etching the oxide layer to create side spacers (fig. 3:7, 17) on each side of the poly gate; and using the third reticle to create a

pattern for heavily doping with the second dopant the active region between the LOCOS regions and the side spacers (page 8, 2nd paragraph). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Uchida with the AAPA in order to establish a CMOS and BICMOS device structures (page 8, 2nd paragraph)."

Applicant's Response

The combination of figure 14 with AAPA would not have been obvious to one of ordinary skill in the art because AAPA defines the structure for a single cell. Figure 14 and the elements relied on therein covered a plurality of transistor elements, whereas AAPA teaches forming a single memory cell. Therefore, the combinations of the plurality of steps used to manufactured different circuit elements with a single element would not have been obvious to one of ordinary skill in the art. However, one of ordinary skill in the art would understand that a memory contains many memory cells all manufactured with the same process.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 14, Uchida discloses wherein the process according to claim 1, further including the step of: implanting the second type of dopant into the semiconductor substrate prior to the step of growing the epitaxial layer (page 4, paragraph [0063] and fig. 1)."

Applicant's Response

Applicant has distinguished his invention over the Uchida reference as well as the combination of Uchida with AAPA. Therefore, claim 14 provides further definition of what Applicant regards as his invention, and should be allowed for at least the same reasons as claim 13.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 15, Uchida discloses wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant (page 6, paragraph [0079]-[0084] and fig. 1)."

Applicant's Response

Applicant has distinguished his invention over the Uchida reference as well as the combination of Uchida with AAPA. Therefore, claim 15 provides further definition of what Applicant regards as his invention and should be allowed for at least the same reasons as claims 13 and 14.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 17, Uchida discloses wherein the first type of dopant is a P type dopant and the step of lightly doping the second type of dopant between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant wherein each of the first and second lightly doped regions are in contact with the first and second regions (page 6, paragraph [0079]-[0084] and fig. 14)."

Applicant's Response

The element referred to in the rejection is the claimed lightly doped drain regions. Applicant can not identify any such regions in figure 14. Buried N-type layers 61 and 62 are formed in the inside of the substrate and not within the P-well 16 and are not in contact with the lightly doped regions.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 18, Uchida discloses wherein the step of implanting a heavily doping with the second dopant comprises the step of: implanting the heavy dose of N type dopant into the first and second lightly doped regions (page 6, paragraph [0079]-[0084] and fig. 14)."

Applicant's Response

Applicant could not find anywhere in figure 14, on page 6 paragraphs 79-84, the step of implanting the heavy dose of N-type dopant into the first and second lightly doped regions. Thus, claim 18 would not have been obvious to one of ordinary skill in the art.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 19, Uchida discloses wherein the step of: patterning the poly semiconductor layer to create a poly gate (fig. 14:29) includes the step of: patterning the poly gate over the first and second regions (fig. 14)."

Applicant's Response

Figure 14 fails to teach patterning the poly gate over the first and second regions. The references discloses multiple gates over each region and not a single gate over both regions.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 20, Uchida wherein the step of: patterning the first reticle to create a pattern for lightly doping with the second dopant the active region between the LOCOS regions and the poly gate comprises the step of: implanting a light dose of N type dopant (fig. 14)."

Applicant's Response

There is no teaching of a second type of dopant between the locos regions as there are no locos regions shown. Applicant has distinguished independent claim 13 to which claim 20 depends over the cited references. Thus claim 20 should be allowed for at least the same reasons as those discussed in conjunction with claim 13.

Claim Rejections - 35 USC § 103
(Continued)

"In re claim 21, Uchida discloses wherein the step of: using the first reticle to create a pattern for heavily doping between the LOCOS regions and the poly gate comprises the step of: implanting a heavy dose of N type dopant (fig. 14)."

Applicant's Response

Applicant has previously distinguished independent claim over the combination of Uchida and AAPA. Claim 21 provides further definition of the steps used to practice Applicant's inventions and should be allowed for at least the same reasons as those discussed in conjunction with claim 1.

Conclusion

The reference to Uchida (US Pub. 2002/0031882) and in particular figure 14 is not combinable with Applicant's Admitted Prior Art (AAPA) because the admitted prior art describes a single memory cell whereas figure 14 has many circuits. For example, in Uchida the trench isolation 2 referred to in the Official Action only partially isolates the input/output circuit zone 32. Reference may be made to paragraph 0086. According to the referenced paragraph, there are 3 isolation regions and the identified active region would be located within the input/output zone 32. Therefore, only the second region 62 is located within the defined active region. This is contrary to independent claims 1 and 13. The first region 61 is located within the 31 peripheral circuit zone and isolated from the input/output zone 32. Therefore, one cannot combine the teachings of AAPA with the cited reference because one teaches a single active region and the other teaches multiple isolation regions. One of ordinary skill in the art would not even consider the cited reference and could not reduce the combination to practice if considered without undue experimentation.

The claims being in condition for allowance this action is requested.

Respectfully submitted,

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Richard K. Robinson (PTO Reg. No. 28,109)
Harry C. Post, III (PTO Reg. No. 26,019)
Attorneys for Applicant

ROBINSON & POST, LLP
12900 Preston Road, Suite 575
Dallas, Texas 75230
Tel: (972) 866-7786
Fax: (972) 866-7787